PATENT
Attorney Docket No. 401440

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

KOSAKI et al.

Application No.	Unassigned	Art Unit:	Unassigned
Filed:	November 8, 2001	Examiner:	Unassigned
For:	METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE AND SEMI-CONDUCTOR		

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D. C. 20231

Dear Sir:

Prior to the examination of the above-identified patent application, please enter the following amendments and consider the following remarks.

IN THE TITLE:

Replace the title with:

SEMCONDUCTOR DEVICE

IN THE DRAWINGS:

The Examiner is requested to approve the changes to Figures 2F-9L as indicated in the attached Request for Approval of Drawing Amendments.

IN THE SPECIFICATION:

Replace the paragraph beginning at page 1, line 5, with:

The present invention relates to a method for manufacturing a semiconductor device and the semiconductor device manufactured by the method, in which the semiconductor device is manufactured by laser cutting a plate having a number of such semiconductor devices.

Replace to the paragraph beginning at page 1, line 19, with:

PCT/WO98/13862 discloses a method for manufacturing a GaAs high power semiconductor device having such heat radiation metal layer, which is illustrated in Figs. 5A to 5L. According to the method, as shown in Fig. 5A, a first main surface of GaAs substrate 31 carrying semiconductor elements is etched to form a first separation groove 33, in which a photoresist layer 32 provided on the first main surface is used as a mask. Then, as shown in Fig. 5B, the first separation groove 33 is plated with a first metal layer 34. As shown in Fig. 5C, the GaAs substrate 31 then has wax 35 applied on the first main surface and is further bonded onto a supporting wafer 36 made of glass or sapphire. Also, the GaAs substrate 31 is polished at its second main surface to reduce its thickness to about 20 to 30μm. Subsequently, as shown in Fig. 5D, the GaAs substrate 31 is provided at its second main surface with a photoresist layer 44 which is then patterned with an aperture opposing the first separation groove 33. The photoresist layer 44 so patterned is used as a mask for an etching in which the second main surface of the GaAs substrate 31 is etched to the extent that the bottom surface of the first metal layer 34 in the first separation groove 33 is exposed, which results in a second separation groove 63 shown in Fig. 5E.

Replace the paragraph beginning at page 2, line 18, with:

Next, as shown in Fig. 5F, the photoresist layer 44 is removed and then a conducting layer 37 is plated on the entire second main surface of the GaAs substrate 31. Further, as shown in Fig. 5G, a photoresist 45 is provided on the conducting layer 37 which is used for a mask in the subsequent plating of a second metal layer 46 made of the same metal as that of the first metal layer 34. Afterwards, as shown in Fig. 5H, a photoresist layer 47 having a width smaller than that of the second separation groove 63 is formed in the second separation groove 63. With the photoresist layer 47 as a mask, a PHS layer 38 is formed on the second main surface of the GaAs substrate 31 by the 5 electroplating. Next, as shown in Fig. 5I, the GaAs substrate 31 is removed from the supporting wafer 36. In addition, as shown in Fig. 5J, an expandable film 40 is attached on the PHS layer 38. Then, the first and second metal layers, 34 and 46, are grooved and then separated from the first separation groove 33 by exposure to laser light, such as YAG laser light, as illustrated by the dotted line. This results in a semiconductor device shown in Fig. 5K. Finally, as shown in Fig. 5L, the semiconductor device is bonded at its bottom with a package 39 and is provided at its top with bonding wires 40 by a wirebonding technique, and then sealed in a ceramic package or a metal package not shown.

Replace the paragraph beginning at page 9, line 22, with:

Figs. 1A-lK show manufacturing processes for a semiconductor device according to the first embodiment of the present invention;

Replace the paragraphs beginning at page 9, line 25, with:

Figs. Figs. 2A and 2B show manufacturing processes for the semiconductor device according to the first embodiment of the present invention;

Figs. 3A-3C show manufacturing processes for the semiconductor device according to the second embodiment of the present invention;

Fig. 4 shows a manufacturing process for the semiconductor device according to the second embodiment of the present invention; and

Figs. 5A-5L show manufacturing processes for the prior art semiconductor device.

Replace to the paragraph beginning at page 10, line 24, with:

Referring to Figs. 1A to 2B, a method for manufacturing a semiconductor device and a semiconductor device manufactured by the method according to the present invention will be described hereinafter.

Replace the paragraph beginning at page 11, line 3, with:

According to the method, as best shown in Fig. 1A, provided is a GaAs substrate 1 having a semiconductor element in its first main surface. The GaAs substrate 1 is provided on the first main surface with a photoresist layer 2. The layer 2 is used as a mask in a subsequent wet etching process in which the GaAs substrate 1 is etched to form a first separation groove (a surface separation 10 groove) la. Then, a catalyst layer 3 including palladium (Pd) is deposited on an entire surface of the remaining photoresist layer 2 by a suitable film forming technique such as evaporation and sputtering deposition. In this film formation, a part of the catalyst layer 3 is formed on a surface of the first separation groove la.

Replace the paragraph beginning at page 11, line 16, with:

The palladium included in the catalyst layer 3 exists in a considerably stable state so that it never elutes from the catalyst layer 3 to result in an unwanted separation of the catalyst layer 3 in a subsequent formation of the second separation layer lb (see Fig. 1I), which would otherwise be caused if the eluted palladium forms an oxide between the catalyst layer 3 and the GaAs substrate 1.

Replace the paragraph beginning at page 11, line 24, with:

It should be noted that the possible separation of the catalyst layer 3 will result in an unevenness in thickness of a metal layer 10 to be formed on the bottom surface of the catalyst layer 3 and then cut by an exposure to laser light. Also, the unevenness can make defects in the laser cutting in a separation process of the semiconductor devices (see Fig. 1K), which decreases the yield of the semiconductor device. Contrary to this, the catalyst layer 3 so formed will increase the yield of the device.

Replace the paragraph beginning at page 12, line 8, with:

Referring next to Fig. 1B, the catalyst layer 3 on the photoresist layer 2 is removed using a lift off method, except in the first separation groove la.

Replace the paragraph beginning at page 12, line 12, with:

It should be noted that the catalyst layer 3 is a single layer made of palladium, having a thickness of about 10 nm. Preferably, the thickness of the palladium layer is in the range of about 5 to 30 nm. Alternatively, the catalyst layer 3 may be made from layers of palladium and titanium. In this instance, the palladium layer should overlie the titanium layer so that the catalyst layer 3 serves as a catalyst.

Replace the paragraph beginning at page 12, line 20, with:

Referring next to Fig. 1C, a photoresist layer 22 is formed on the substrate 1 so that it does not cover the first separation groove la. As can be seen from the drawing, edges of the photoresist layer 22 extend slightly into the first separation groove la, so that slanted side surfaces defining a part of the first separation groove la are half (about 50%) covered by the photoresist 22.

Replace the paragraph beginning at page 13, line 2, with:

Also, the GaAs substrate 1 is dipped in a nickel (Ni) based electroless plating solution (not shown), for example, Ni-P plating solution. This step assures that, as shown in Fig. 1D, a nickel plating layer 4 is formed only in the first separation groove la.

Replace the paragraph beginning at page 13, line 7, with:

In this nickel based electroless plating, atomic hydrogen serving as a catalyst of reducing reaction and molecular hydrogen giving a stirring effect, generated in the plating reaction, improve the formation of the plating film.

Replace the paragraph beginning at page 13, line 20, with:

This means that, in the first separation groove la, a hypophosphorous acid ion in the plating solution is dissolved as indicated by the equation 1 using palladium contained in the catalyst layer 3 as a catalyst. This supplies enough atomic hydrogen to the side walls of the first separation groove la. At the side walls of the first separation groove la, an electron is carried away from nickel ion in the side wall, so that the nickel ion is reduced as shown by the equation 3, whereby nickel is deposited. Phosphorus (P) is also deposited from hypophosphorous acid ion as indicated by the equation 4. Thereby, a nickel based plating layer 4 (a Ni-P alloy plating layer) is formed on the bottom of the first separation groove la. Further, some atomic hydrogen is supplied to portions of the side walls of the first separation groove la, away from the catalyst layer 3. This results in, as shown in Fig. 1D, the nickel based plating layer 4 being formed so that it extends from the surface of the catalyst layer 3 onto the side walls.

Replace the paragraph beginning at page 14, line 14, with:

On the other hand, the second main surface and a is peripheral surface of the GaAs substrate 1 are far away from the catalyst layer 3 which is a source of the atomic hydrogen, so that hydrogen is not supplied to the surfaces. Therefore, no plating layer is

formed on the second main surface or the peripheral surface of the GaAs substrate 1. This means that, by using this method, the nickel based plating layer 4 can be formed selectively only near the catalyst layer 3 to which the atomic hydrogen can be supplied. This, in turn, allows that the topmost of the nickel based plating layer 4 to be located below that of the opening of the first separation groove la, which ensures that no short circuit would occur between the plating layer 4 and the bonding wire at the wirebonding of the GaAs substrate 1.

Replace the paragraph beginning at page 15, line 4, with:

Furthermore, although the nickel based plating layer 4 is formed using the catalyst layer 3, it may be provided only by electroless plating. In this instance, the GaAs substrate 1 must be dipped in a solution containing phosphorus before the electroless plating in order to form a catalyst nucleus in the first separation groove la. This plating may have some drawbacks.

Replace the paragraph beginning at page 15, line 11, with:

Specifically, phosphorus ion may deposit on a portion on which the nickel based plating layer should not be formed, for example, the upper surface of the photoresist layer and the second main surface of the GaAs substrate 1. This undesired deposition may result in the nickel based plating layer being formed on the second main surface of the GaAs substrate 1 in the electroless plating.

Replace the paragraph beginning at page 15, line 18, with:

Also, the nickel based plating layer grown on the photoresist layer disadvantageously may in part separate into a solvent in a process for removing the photoresist (see Fig. 1E), so the separated plating layer adheres again to the surface of the GaAs substrate 1 in the subsequent processes, which provides an adverse effect.

Replace the paragraph beginning at page 15, line 25, with:

Further, the nickel based plating layer formed on the second main surface of the GaAs substrate 1 may result in a variation of the etching of the second main surface of the GaAs substrate 1 in a thinning process of the GaAs substrate 1 (Fig. 1F), causing an unevenness in thickness of the etched GaAs substrate 1. In addition, the nickel based plating layer formed on the peripheral surface of the GaAs substrate 1 may result in binding in a polishing blade at the thinning process, which may crack or damage the GaAs substrate.

Replace the paragraph beginning at page 16, line 12, with:

Next, as shown in Fig. 1F, the first main surface of the GaAs substrate 1 is coated with a wax 5 as an adhesive through which a supporting wafer 6 is. bonded on the substrate 1. The supporting wafer 6 is a plate made of suitable material such as glass and sapphire. Then, the GaAs substrate 1 is thinned from its second main surface to about 20 to 30μm. The thinning may be accomplished by any suitable manner such as grinding, lapping, and polishing.

Replace the paragraph beginning at page 16, line 20, with:

Next, as shown in Fig. 1G, the entire second main surface of the GaAs substrate 1 is coated with a first conducting layer 7. The conducting layer 7 may be formed by, for example, forming a nickel based plating layer on the first main surface of the GaAs substrate 1, and substituting the upper surface of the plating layer for gold (Au). Then, a part of the second main surface of the GaAs substrate 1, opposing the first separation groove 1a, is formed with a photoresist layer (not shown). Preferably, a width of the photoresist layer is smaller than that of the groove 1a. The photoresist layer is used as a mask in an electrolytic process in which a PHS layer 8 made from gold is formed on the conducting layer 7. Then, the photoresist layer is removed.

Replace the paragraph beginning at page 17, line 9, with:

As shown in Fig. 1H, the PHS layer 8 serves as a mask in an etching process in which a portion of the conducting layer 7 adjacent to the groove la is removed. This etching process is extended to the lower surface of the catalyst layer 3 to form a second separation groove lb.

Replace the paragraph beginning at page 17, line 14, with:

Next, as shown in Fig. 1I, a second conducting layer 9 is formed on surfaces of the second separation groove lb and the PHS layer 8 by electroless plating, similar to the first conducting layer 7. The process for forming the second conducting layer 9 may be the same as that for the first conducting layer 7. Further, a metal layer 10 is formed on the second conducting layer 9 by the electroplating process. Preferably, the metal layer 10 is made of a metal having a melting point higher than that of the nickel based plating layer 4 in the first separation groove la and having a reflection ratio of less than 8% of YAG laser light. Also preferably, the nickel based plating layer 4 is made from nickel based alloy selected from materials such as Ni-P, Ni-B and Ni-B-W, and the metal layer 10 is made of material such as nickel and chromium.

Replace the paragraph beginning at page 18, line 4, with:

Referring to Fig. 1J, the entire surfaces of the metal layer 10 and the second separation groove lb are covered by a titanium (Ti) layer about 0.05μm in thickness and then a gold (Au) layer about 0.2-0.3μm in thickness by a suitable film formation technique, such as sputtering deposition and evaporation, forming a Ti/Au layer 11.

Replace the paragraph beginning at page 18, line 10, with:

It should be noted that the Ti/Au layer 11, which improves wettability of the lower surface of the PHS layer 8 against an AuSn solder used for bonding the lower surface of the PHS layer 8 onto the package, can be removed therefrom.

Replace the paragraph beginning at page 18, line 15, with:

Finally, referring to Fig. 1K, the GaAs substrate 1 is removed from the supporting wafer 6. Also, the wax 5 is removed using an organic solvent. Further, an expandable film (not shown) is attached on the PHS layer 8 on the second main surface (back side) of the GaAs substrate 1. Then, the YAG laser beam is irradiated from above, toward the first separation groove la to heat-cut the nickel based plating layer 4, the catalyst layer 3, the second conducting layer 9 having the nickel plating layer and the gold layer, the metal layer 10, and the Ti/Au layer 11 (as shown by a dotted line in Fig. 1K). It should be noted that the expandable film remains uncut, and is expanded in all directions by a suitable expander to separate each element so manufactured from one another. In this way, the GaAs substrate 1 is separated into pieces, each of which forms an independent semiconductor element having the separated piece of the GaAs substrate 1. An example of the semiconductor element or device so manufactured is illustrated in Figs. 2A and 2B.

Replace the paragraph beginning at page 19, line 9, with:

In the semiconductor device so manufactured, the topmost of the nickel based plating layer (metal layer) 4, running around the GaAs substrate 1, is positioned below the first main surface of the GaAs substrate 1. Therefore, when a bonding wire is bonded on the first main surface of the GaAs substrate 1 as shown in Fig. 5L, it is never short circuited to the nickel based plating layer 4, which- increases the production yield of the semiconductor device.

Replace the paragraph beginning at page 19, line 18, with:

As best shown in Fig. 4B, the semiconductor device so manufactured has a peripheral projecting flange 20 running around the substrate 1. The flange includes a plurality of layers; the nickel based plating layer 4 (for example, a Ni-P layer, Ni-B layer, a NI-B-W layer), catalyst layer 3 (for example, a Pd layer, a Pd/Ti layer), nickel based electrolessly plated alloy layer (for example, the Ni-P layer, Ni-B layer, NI-B-W layer) ,

substituted electroless gold plated layer, laser-cut metal layer 10 (for example, a Ni layer, a Cr layer) , gold layer or Ti/Au layer 11. It should be noted that the second conducting layer 9 has a nickel based electroless plating alloy layer and a 5 substituted electrolessly gold plated layer. It should also be noted that the gold layer or the Ti/Au layer 11 may be eliminated as described above.

Replace the paragraph beginning at page 20, line 10, with:

A second embodiment of the present invention will be described below with reference to Fig. 3A through Fig. 4. In this embodiment, processes described with reference to Figs. 1A to 1I in connection with the first embodiment are performed, thereby obtaining an intermediate product shown 15 in Fig 3A. The intermediate product is processed, which will be described below.

Replace the paragraph beginning at page 20, line 17, with:

Referring to Fig. 3B, the entire surface of metal layer 10 is coated with a positive photoresist layer which is then exposed and then developed so that only a part of the layer indicated at 222 remains in the second separation groove lb. Then, a major part of the second conducting layer 9 and the metal layer 10 on the PHS layer 8 is removed by etching or milling, so that a minor part of the second conducting layer 9 and the laser-cut layer 10 still remains in the second separation groove lb.

Replace the paragraph beginning at page 21, line 1, with:

Finally, as shown in Fig. 3C, the remaining photoresist layer 222 is removed using an organic solvent or the like. Then, as described in the first embodiment, the YAG laser light is irradiated from above toward the first separation groove la to cut the nickel based plating layer 4, the catalyst layer 3, the second conducting layer 9, the laser-cut metal layer 10, and then the Ti/Au layer 11. In this way, the GaAs substrate 1 is separated into pieces, each of which forms an independent semiconductor element or device having the

separated piece of the GaAs substrate 1. An example of the semiconductor element or device so manufactured is illustrated in Fig. 4.

Replace the paragraph beginning at page 21, line 13, with:

Similar to the semiconductor device according to the first embodiment, the semiconductor device of this embodiment has a peripheral projecting flange running around the substrate 1. The flange includes a plurality of layers; a nickel based plating layer 4 (for example, the NiP layer, Ni-B layer, NI-B-W layer), a catalyst layer 3 (for example, Pd layer, Pd/Ti layer) , a nickel based electrolessly plated alloy layer (for example, Ni-P layer, Ni-B layer, NI-B-W layer), a substituted electrolessly gold plated layer, and then a laser-cut metal layer 10 (for example, Ni layer, Cr layer). It should be noted that the second conducting layer 9 has a nickel based electrolessly plated alloy layer and a substituted electrolessly gold plated layer.

IN THE CLAIMS

Cancel claim 1-5 and replace the indicated claims with:

6. (Amended) A semiconductor device comprising:

a semiconductor substrate having first and second main surfaces, having a semiconductor element in the first main surface, and having a peripheral surface contacting the first and second main surfaces;

a heat radiation layer on the second main surface of the semiconductor substrate; and

a flange including a plurality of metal layers disposed on the peripheral surface of the substrate, the metal layers comprising:

a first metal layer having a surface layer containing palladium on a side toward the first main surface;

a second metal layer of a nickel-based alloy disposed on the surface layer containing palladium of the first metal layer, the second metal layer having a top portion located below the first main surface; and

a third metal layer disposed under the first metal layer.

7. (Amended) The semiconductor device according to claim 6, wherein the third metal layer comprises a nickel-based alloy layer, a gold layer, and a laser-cut metal layer including one of a nickel layer and a chromium layer.

8. (Amended) The semiconductor device according to claim 7, wherein the third metal layer is selected from the group consisting of a single layer of gold, and a plurality of layers including a titanium layer and a gold layer, on the laser-cut metal layer.

9. (Amended) The semiconductor device according to claim 6, wherein the first metal layer comprises one selected from the group consisting of a palladium layer and a titanium layer under the palladium layer, and a single layer.

10. (Amended) The semiconductor device according to claim 6, wherein the second metal layer is selected from the group consisting of Ni-P alloy, Ni-B alloy, and Ni-B-W alloy.

IN THE ABSTRACT

Replace the abstract with:

ABSTRACT OF THE DISCLOSURE

A semiconductor device having a plated heat sink (PHS) layer on the back surface, preventing a short circuit between a bonding wire, and a first metal layer. A method of making a semiconductor device including forming a catalyst layer on a bottom of a first separation groove in the front surface of a semiconductor substrate, and forming the first metal layer selectively in the first separation groove by electroless plating, using the catalyst layer as a catalyst.

REMARKS

The foregoing amendments are made to correct minor translational errors and to meet United States requirements as to form. No new matter is added.

Respectfully submitted,

LEYDIG, VOIT & MAYER, LTD.

Jeffrey A. Wyand,
Registration No. 29,458

Suite 300
700 Thirteenth Street, N. W.
Washington, D. C. 20005
Telephone: (202) 737-6770
Facsimile: (202) 737-6776
Date: November 8, 2001
JAW:cmcg

PATENT
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In re Application of:

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Application No.	Unassigned	Art Unit:	Unassigned
Filed:	November 8, 2001	Examiner:	Unassigned
For:	METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE AND SEMI-CONDUCTOR		

AMENDMENTS TO SPECIFICATION, CLAIMS, AND ABSTRACT MADE VIA PRELIMINARY AMENDMENT

Amendments to the paragraph beginning at page 1, line 5:

The present invention relates to a method for manufacturing a semiconductor device and the semiconductor device manufactured by the method, in which the semiconductor device is ~~each~~ manufactured by ~~using a~~ laser cutting a plate having a number of such semiconductor devices.

Amendments to the paragraph beginning at page 1, line 19:

PCT/WO98/13862 discloses a method for manufacturing a GaAs high power semiconductor device having such heat radiation metal layer, which is illustrated in Figs. ~~7~~5A to ~~9~~5L. According to the method, as shown in Fig. ~~7~~5A, a first main surface of GaAs substrate 31 carrying semiconductor elements is etched to form a first separation groove 33, in which a photoresist layer 32 provided on the first main surface is used as a mask. Then, as shown in Fig. ~~7~~5B, the first separation groove 33 is plated with a first metal layer 34. As shown in Fig. ~~7~~5C, the GaAs substrate 31 then ~~is~~ has wax 35 applied ~~with a wax 35~~ on the first main surface and is further bonded onto a supporting wafer 36

made of glass or sapphire. Also, the GaAs substrate 31 is polished at its second main surface to reduce its thickness to about 20 to 30μm. Subsequently, as shown in Fig. ~~7~~5D, the GaAs substrate 31 is provided at its second main surface with a photoresist layer 44 which is then patterned with an aperture opposing ~~to~~ the first separation groove 33. The photoresist layer 44 so patterned is used as a mask for an etching in which the second main surface of the GaAs substrate 31 is etched to the extent that the bottom surface of the first metal layer 34 in the first separation groove 33 ~~would expose~~ is exposed, which results in a second separation groove 63 shown in Fig. ~~8~~5E.

Amendments to the paragraph beginning at page 2, line 18:

Next, as shown in Fig. ~~8~~5F, the photoresist layer 44 is removed and then a conducting layer 37 is plated on the entire second main surface of the GaAs substrate 31. Further, as shown in Fig. ~~8~~5G, a photoresist 45 is provided on the conducting layer 37 which is used for a mask in the subsequent plating of a second metal layer 46 made of the same metal as that of the first metal layer 34. Afterwards, as shown in Fig. ~~8~~5H, a photoresist layer 47 having a width smaller than that of the second separation groove 63 is formed in the second separation groove 63. With the photoresist layer 47 as a mask, a PHS layer 38 is formed on the second main surface of the GaAs substrate 31 by the 5 electroplating. Next, as shown in Fig. ~~9~~5I, the GaAs substrate 31 is removed from the supporting wafer 36. In addition, as shown in Fig. ~~9~~5J, an expandable film 40 is attached on the PHS layer 38. Then, the first and second metal layers, 34 and 46, are grooved and then separated from the first separation groove 33 by ~~the~~ exposure ~~of~~ to laser light, such as YAG laser light, as illustrated by the dotted line. This results in a semiconductor device shown in Fig. ~~9~~5K. Finally, as shown in Fig. ~~9~~5L, the semiconductor device is bonded at its bottom with a package 39 and is provided at its top with bonding wires 40 by a wirebonding technique, and then sealed in a ceramic package or a metal package not shown.

Amendments to the paragraph beginning at page 9, line 22:

Figs. 1A-l~~E~~K show manufacturing processes for a semiconductor device according to the first embodiment of the present invention;

Amendments to the paragraphs beginning at page 9, line 25:

~~Figs. 2F-2G show manufacturing processes for the semiconductor device according to the first embodiment of the present invention;~~

~~Figs. 3I-3K show manufacturing processes for the semiconductor device according to the first embodiment of the present invention;~~

Figs.~~4A-4B~~ Figs. 2A and 2B show manufacturing processes for the semiconductor device according to the first embodiment of the present invention;

Figs.~~5A-5C~~ 3A-3C show manufacturing processes for the semiconductor device according to the second embodiment of the present invention;

Fig. ~~6~~4 shows a manufacturing process for the semiconductor device according to the second embodiment of the present invention;

~~Figs. 7A-7D show manufacturing processes for a prior art semiconductor device;~~

~~Figs. 8E-8H show manufacturing processes for the prior art semiconductor device;~~

and

Figs.~~9I-9L~~ 5A-5L show manufacturing processes for the prior art semiconductor device.

Amendments to the paragraph beginning at page 10, line 24:

Referring to Figs. 1A to ~~4~~2B, a method for manufacturing a semiconductor device and a semiconductor device manufactured by the method according to the present invention will be described hereinafter.

Amendments to the paragraph beginning at page 11, line 3:

According to the method, as best shown in Fig. 1A, provided is a GaAs substrate 1 having a semiconductor element in its first main surface. The GaAs substrate 1 is provided on the first main surface with a ~~photoresist~~ photoresist layer 2. The layer 2 is used as a mask in a subsequent wet etching process in which the GaAs substrate 1 is etched to form a first separation groove (a surface separation 10 groove) la. Then, a catalyst layer 3 including palladium (Pd) is deposited on an entire surface of the remaining photoresist layer 2 by a suitable film forming technique such as evaporation and sputtering deposition. In this film formation, a part of the catalyst layer 3 is formed on a surface of the first separation groove la.

Amendments to the paragraph beginning at page 11, line 16:

The palladium included in the catalyst layer 3 exists in a considerably stable state so that it never ~~elute out of~~ elutes from the catalyst layer 3 to result in an unwanted separation of the catalyst layer 3 in a subsequent formation of the second separation layer lb (see Fig. ~~3~~1I), which would otherwise be caused ~~by that~~ if the eluted palladium forms an oxide between the catalyst layer 3 and the GaAs substrate 1.

Amendments to the paragraph beginning at page 11, line 24:

It should be noted that the possible separation of the catalyst layer 3 will result in an unevenness in thickness of a metal layer 10 to be formed on the bottom surface of the catalyst layer 3 and then cut by an exposure ~~of~~ to laser light. Also, the unevenness can make defects in the laser cutting in a separation process of the semiconductor devices (see Fig. ~~3~~1K), which decreases the yield of the semiconductor device. Contrary to this, the catalyst layer 3 so formed will increase the yield of the device.

Amendments to the paragraph beginning at page 12, line 8:

Referring next to Fig. 1B, the catalyst layer 3 on the photoresist layer 2 is removed using a lift off method, except ~~for that exists~~ in the first separation groove 1a.

Amendments to the paragraph beginning at page 12, line 12:

It should be noted that the catalyst layer 3 is a single layer made of palladium, having a thickness of about 10 nm. Preferably, the thickness of the palladium layer is in the range of about 5 to 30 nm. Alternatively, the catalyst layer 3 may be made from ~~two~~ layers of palladium and titanium. In this instance, the palladium layer should overlie the titanium layer so that the catalyst layer 3 serves as a catalyst.

Amendments to the paragraph beginning at page 12, line 20:

Referring next to Fig. 1C, a photoresist layer 22 is formed on the substrate 1 so that it does not cover the first separation groove 1a. As can be seen from the drawing, edges of the photoresist layer 22 ~~extends~~ extend slightly into the first separation groove 1a, so that slanted side surfaces defining a part of the first separation groove 1a ~~is~~ are half (about 50%) covered by the photoresist 22.

Amendments to the paragraph beginning at page 13, line 2:

Also, the GaAs substrate 1 is dipped in a nickel (Ni) based electroless plating solution (not shown), for example, Ni-P plating solution. This ~~allows~~ step assures that, as shown in Fig. 1D, a nickel plating layer 4 is formed only in the first separation groove 1a.

Amendments to the paragraph beginning at page 13, line 7:

In this nickel based electroless plating, atomic hydrogen serving as a catalyst of reducing reaction and molecular hydrogen giving a stirring effect, generated in the plating reaction, improve the formation of the plating film.

Amendments to the paragraph beginning at page 13, line 20:

This means that, in the first separation groove 1a, a hypophosphorous acid ion in the plating solution is dissolved as indicated by the equation 1 using palladium contained in the catalyst layer 3 as a catalyst. This supplies enough atomic hydrogen to the side walls of the first separation groove 1a. At the side walls of the first separation groove 1a, an electron is carried away from nickel ion in the side wall, so that the nickel ion is reduced as shown by the equation 3, ~~thereby~~ whereby nickel is deposited. Phosphorus (P) is also deposited from hypophosphorous acid ion as indicated by the equation 4. Thereby, a nickel based plating layer 4 (a Ni-P alloy plating layer) is formed on the bottom of the first separation groove 1a. Further, some atomic hydrogen is supplied to portions of the side walls of the first separation groove 1a, away from the catalyst layer 3. This results in ~~that~~, as shown in Fig. 1D, the nickel based plating layer 4 ~~is~~ being formed so that it extends from the surface of the catalyst layer 3 onto the side walls.

Amendments to the paragraph beginning at page 14, line 14:

On the other hand, the second main surface and a is peripheral surface of the GaAs substrate 1 are far away from the catalyst layer 3 which is a source of the atomic hydrogen, so that hydrogen is not supplied to the surfaces. Therefore, no plating layer is formed on the second main surface or the peripheral surface of the GaAs substrate 1. This means that, by using this method, the nickel based plating layer 4 can be formed selectively only near the catalyst layer 3 to which the atomic hydrogen can be supplied. This, in turn, allows that the topmost of the nickel based plating layer 4 ~~is~~ to be located below that of the opening of the first separation groove 1a, which ensures that no short circuit would occur between the plating layer 4 and the bonding wire at the wirebonding of the GaAs substrate 1.

Amendments to the paragraph beginning at page 15, line 4:

Furthermore, although the nickel based plating layer 4 is formed using the catalyst layer 3, it may be provided only ~~an~~ by electroless plating. In this instance, the GaAs substrate 1 ~~is needed to dip~~ must be dipped in a solution containing phosphorus before the electroless plating in order to form a catalyst nucleus in the first separation groove 1a. This plating may have some drawbacks.

Amendments to the paragraph beginning at page 15, line 11:

Specifically, phosphorus ion may deposit on a portion on which the nickel based plating layer should not be formed, for example, the upper surface of the photoresist layer and the second main surface of the GaAs substrate 1. This undesired deposition may result in ~~that~~ the nickel based plating layer ~~is~~ being formed on the second main surface of the GaAs substrate 1 in the electroless plating.

Amendments to the paragraph beginning at page 15, line 18:

Also, the nickel based plating layer grown on the photoresist layer disadvantageously may in part separate into a solvent in a process for removing the photoresist (see Fig. 1E), ~~and~~ so the separated plating layer adheres again to the surface of the GaAs substrate 1 in the subsequent processes, which provides an adverse ~~affect~~ effect.

Amendments to the paragraph beginning at page 15, line 25:

Further, the nickel based plating layer formed on the second main surface of the GaAs substrate 1 may result in a variation of the etching of the second main surface of the GaAs substrate 1 in a thinning process of the GaAs substrate 1 (Fig. ~~2~~1F), causing an unevenness in thickness of the etched GaAs substrate 1. In addition, the nickel based plating layer formed on the peripheral surface of the GaAs substrate 1 may result in ~~a blinding~~ binding in a polishing blade at the thinning process, which may crack or damage the GaAs substrate.

Amendments to the paragraph beginning at page 16, line 12:

Next, as shown in Fig. ~~2~~1F, the first main surface of the GaAs substrate 1 is coated with a wax 5 as an adhesive through which a supporting wafer 6 is. bonded on the substrate 1. The supporting wafer 6 is a plate made of suitable material such as glass and sapphire. Then, the GaAs substrate 1 is thinned from its second main surface to about 20 to 30μm. The thinning may be accomplished by any suitable manner such as grinding, ~~rapping~~ lapping, and polishing.

Amendments to the paragraph beginning at page 16, line 20:

Next, as shown in Fig. ~~2~~1G, the entire second main surface of the GaAs substrate 1 is coated with a first conducting layer 7. The conducting layer 7 may be formed by, for example, forming a nickel based plating layer on the first main surface of the GaAs substrate 1, and substituting the upper surface of the plating layer for gold (Au). Then, a part of the second main surface of the GaAs substrate 1, opposing ~~to~~ the first separation groove la, is formed with a photoresist layer (not shown). Preferably, a width of the photoresist layer is smaller than that of the groove la. The ~~phtoresist~~ photoresist layer is used as a mask in an electrolytic process in which a PHS layer 8 made from gold is formed on the conducting layer 7. Then, the photoresist layer is removed.

Amendments to the paragraph beginning at page 17, line 9:

As shown in Fig. ~~2~~1H, the PHS layer 8 serves as a mask in an etching process in which a portion of the conducting layer 7 adjacent to the groove la is removed. This etching process is extended to the lower surface of the catalyst layer 3 to form a second separation groove lb.

Amendments to the paragraph beginning at page 17, line 14:

Next, as shown in Fig. ~~3~~1I, a second conducting layer 9 is formed on surfaces of the second separation groove lb and the PHS layer 8 by ~~the~~ electroless plating, similar to the first conducting layer 7. The process for forming the second conducting layer 9 may be the same as that for the first conducting layer 7. Further, a metal layer 10 is formed on the second conducting layer 9 by the electroplating process. Preferably, the metal layer 10 is made of a metal having a melting point higher than that of the nickel based plating layer 4 in the first separation groove la and having a reflection ratio of less than 8% ~~against the~~ of YAG laser light. Also preferably, the nickel based plating layer 4 is made from nickel based alloy selected from materials such as Ni-P, Ni-B and Ni-B-W, and the metal layer 10 is made of material such as nickel and chromium.

Amendments to the paragraph beginning at page 18, line 4:

Referring to Fig. ~~3~~1J, the entire surfaces of the metal layer 10 and the second separation groove lb are covered by a titanium (Ti) layer about 0.05μm in thickness and then a gold (Au) layer about 0.2-0.3μm in thickness by a suitable film formation technique, such as sputtering deposition and evaporation, forming a Ti/Au layer 11.

Amendments to the paragraph beginning at page 18, line 10:

It should be noted that the Ti/Au layer 11, which improves ~~a~~ wettability of the lower surface of the PHS layer 8 against an AuSn solder used for bonding the lower surface of the PHS layer 8 onto the package, can be removed therefrom.

Amendments to the paragraph beginning at page 18, line 15:

Finally, referring to Fig. ~~3~~1K, the GaAs substrate 1 is removed from the supporting wafer 6. Also, the wax 5 is removed using an organic solvent. Further, an expandable film (not shown) is attached on the PHS layer 8 on the second main surface (back side) of the GaAs substrate 1. Then, the YAG laser beam is irradiated from above,

toward the first separation groove la to heat-cut the nickel based plating layer 4, the catalyst layer 3, the second conducting layer 9 having the nickel plating layer and ~~then~~ the gold layer, the metal layer 10, and the Ti/Au layer 11 (as shown by a dotted line in Fig. ~~3~~1K). It should be noted that the expandable film remains uncut, ~~which~~ and is expanded in all directions by a suitable expander to separate each element so manufactured from one another. In this way, the GaAs substrate 1 is separated into pieces, each of which forms an independent semiconductor element having the separated piece of the GaAs substrate 1. An example of the semiconductor element or device so manufactured is illustrated in Figs. ~~4~~2A and ~~4~~2B.

Amendments to the paragraph beginning at page 19, line 9:

In the semiconductor device so manufactured, the topmost of the nickel based plating layer (metal layer) 4, running around the GaAs substrate 1, ~~positions~~ is positioned below the first main surface of the GaAs substrate 1. Therefore, when a bonding wire is bonded on the first main surface of the GaAs substrate 1 as shown in Fig. ~~9~~5L, it ~~would~~ is never ~~make a~~ short ~~circuit with~~ circuited to the nickel based plating layer 4, which increases the production yield of the semiconductor device.

Amendments to the paragraph beginning at page 19, line 18:

As best shown in Fig. 4B, the semiconductor device so manufactured has a peripheral ~~projected~~ projecting flange 20 running around the substrate 1. The flange includes a plurality of layers; the nickel based plating layer 4 (for example, a Ni-P layer, Ni-B layer, a NI-B-W layer), catalyst layer 3 (for example, a Pd ~~later~~ layer, a Pd/Ti layer), nickel based ~~electroless plating~~ electrolessly plated alloy layer (for example, the Ni-P layer, Ni-B layer, NI-B-W layer) , substituted electroless gold ~~plating~~ plated layer, laser-cut metal layer 10 (for example, a Ni layer, a Cr layer) , gold layer or Ti/Au layer 11. It should be noted that the second conducting layer 9 has a nickel based electroless plating alloy layer and a 5 substituted electrolessly gold ~~plating~~ plated layer. It should also be noted that, the gold layer or the Ti/Au layer 11 may be eliminated as described above.

Amendments to the paragraph beginning at page 20, line 10:

A second embodiment of the present invention will be described below with reference to Fig. ~~5~~3A through Fig.~~6~~ 4. In this embodiment, processes described with reference to Figs. 1A to ~~3~~1I in connection with the first embodiment are performed, thereby ~~obtained~~ obtaining an intermediate product shown 15 in Fig ~~5~~3A. The intermediate product is processed, which will be described below.

Amendments to the paragraph beginning at page 20, line 17:

Referring to Fig. ~~5~~3B, the entire surface of metal layer 10 is coated with a positive photoresist layer which is then exposed and then developed so that only a part of the layer indicated at 222 remains in the second separation groove lb. Then, a major part of the second conducting layer 9 and the metal layer 10 on the PHS layer 8 is removed by etching or milling, so that a minor part of the second conducting layer 9 and the laser-cut layer 10 still remains in the second separation groove lb.

Amendments to the paragraph beginning at page 21, line 1:

Finally, as shown in Fig. ~~5~~3C, the remaining photoresist layer 222 is removed using an organic solvent or the like. Then, as described in the first embodiment, the YAG laser light is irradiated from above toward the first separation groove la to cut the nickel based plating layer 4, the catalyst layer 3, the second conducting layer 9, the laser-cut metal layer 10, and then the Ti/Au layer 11. In this way, the GaAs substrate 1 is separated into pieces, each of which forms an independent semiconductor element or device having the separated piece of the GaAs substrate 1. An example of the semiconductor element or device so manufactured is illustrated in Fig.~~6~~ 4.

Amendments to the paragraph beginning at page 21, line 13:

Similar to the semiconductor device according to the first embodiment, the semiconductor device of this embodiment has a peripheral ~~projected~~ projecting flange running around the substrate 1. The flange includes a plurality of layers; a nickel based plating layer 4 (for example, the NiP layer, Ni-B layer, NI-B-W layer), a catalyst layer 3 (for example, Pd ~~later~~ layer, Pd/Ti layer) , a nickel based ~~electroless plating~~ electrolessly plated alloy layer (for example, Ni-P layer, Ni-B layer, NI-B-W layer), a substituted ~~electroless~~ electrolessly gold ~~plating~~ plated layer, and then a laser-cut metal layer 10 (for example, Ni layer, Cr layer). It should be noted that the second conducting layer 9 has a nickel based ~~electroless plating~~ electrolessly plated alloy layer and a substituted electrolessly gold ~~plating~~ plated layer.

Amendments to the existing claims:

6. (Amended) A semiconductor device comprising:

a semiconductor substrate having first and second main surfaces, having a semiconductor element ~~formed~~ in the first main surface, and having a peripheral surface ~~containing~~ contacting the first and second main ~~surface~~ surfaces;

a heat radiation layer ~~provided~~ on the second main surface of the semiconductor substrate; and

a flange ~~of~~ including a plurality of metal layers disposed on the peripheral surface of the substrate, the metal layers comprising ~~;~~:

a first metal layer having a surface layer containing palladium on ~~the same~~ a side ~~with~~ toward the first main surface;

a second metal layer of a nickel-based alloy disposed on the surface layer containing palladium of the first metal layer, ~~and~~ the second metal layer having a top portion located ~~at a distance~~ below the first main surface; and

a third metal layer disposed under the first metal layer.

7. (Amended) ~~A~~The semiconductor device according to claim 6, wherein the third metal layer comprises a nickel-based alloy layer, a gold layer, and a laser-cut metal layer including one of a nickel layer ~~or~~ and a chromium layer.

8. (Amended) ~~A~~The semiconductor device according to claim 7, wherein the third metal layer ~~comprises~~ is selected from the group consisting of a single layer of gold ~~or~~, and a plurality of layers including a titanium layer and a gold layer, on the laser-cut metal layer.

9. (Amended) ~~A~~The semiconductor device according to claim 6, wherein the first metal layer comprises ~~two layers of~~ one selected from the group consisting of a palladium layer and a titanium layer under the palladium layer, ~~or~~ and a single layer.

10. (Amended) ~~A~~The semiconductor device according to claim 6, wherein the second metal layer is ~~made of one material~~ selected from the group consisting of Ni-P alloy, Ni-B alloy, ~~or~~ and Ni-B-W alloy.

Amendments to the abstract:

ABSTRACT OF THE DISCLOSURE

A semiconductor device having a plated heat sink (PHS) layer on the back surface ~~thereof~~, preventing ~~from~~ a short circuit between a bonding wire, and a first metal layer. ~~Forming~~A method of making a semiconductor device including forming a catalyst layer on a bottom of a first separation groove ~~formed~~ in the front surface of a semiconductor substrate, and forming the first metal layer selectively in the first separation groove by ~~an~~ electroless plating ~~technique~~, using the catalyst layer as a catalyst.

PATENT
Attorney Docket No. 401440

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

KOSAKI et al.

Application No.	Unassigned	Art Unit:	Unassigned
Filed:	November 8, 2001	Examiner:	Unassigned
For:	METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE AND SEMI-CONDUCTOR		

PENDING CLAIMS AFTER ENTRY OF PRELIMINARY AMENDMENT

6. A semiconductor device comprising:

a semiconductor substrate having first and second main surfaces, having a semiconductor element in the first main surface, and having a peripheral surface contacting the first and second main surfaces;

a heat radiation layer on the second main surface of the semiconductor substrate; and

a flange including a plurality of metal layers disposed on the peripheral surface of the substrate, the metal layers comprising:

a first metal layer having a surface layer containing palladium on a side toward the first main surface;

a second metal layer of a nickel-based alloy disposed on the surface layer containing palladium of the first metal layer, the second metal layer having a top portion located below the first main surface; and

a third metal layer disposed under the first metal layer.

7. The semiconductor device according to claim 6, wherein the third metal layer comprises a nickel-based alloy layer, a gold layer, and a laser-cut metal layer including one of a nickel layer and a chromium layer.

8. The semiconductor device according to claim 7, wherein the third metal layer is selected from the group consisting of a single layer of gold, and a plurality of layers including a titanium layer and a gold layer, on the laser-cut metal layer.

9. The semiconductor device according to claim 6, wherein the first metal layer comprises one selected from the group consisting of a palladium layer and a titanium layer under the palladium layer, and a single layer.

10. The semiconductor device according to claim 6, wherein the second metal layer is selected from the group consisting of Ni-P alloy, Ni-B alloy, and Ni-B-W alloy.

PATENT
Attorney Docket No. 401440

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Filed:	November 8, 2001	Examiner:	Unassigned
For:	METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE AND SEMI-CONDUCTOR		

REQUEST FOR APPROVAL OF DRAWING AMENDMENT

Commissioner for Patents
Washington, D. C. 20231

Dear Sir:

The Examiner is requested to approve the changes indicated in red on the attached copies of Figures 2F-9L.

Respectfully submitted,

LEYDIG, VOIT & MAYER, LTD.

Jeffrey A. Wyand,
Registration No. 29,458

Suite 300
700 Thirteenth Street, N. W.
Washington, D. C. 20005
Telephone: (202) 737-6770
Facsimile: (202) 737-6776
Date: November 5, 2001
JAW:cmcg

Fig. ~~2~~1F

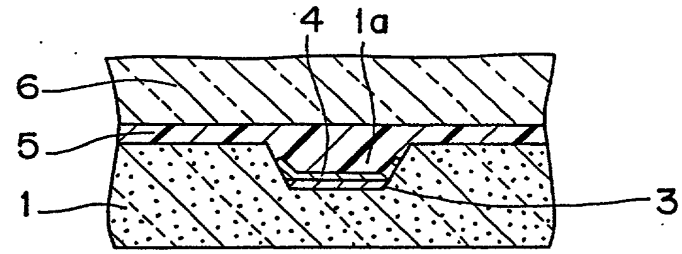

Fig. ~~2~~1G

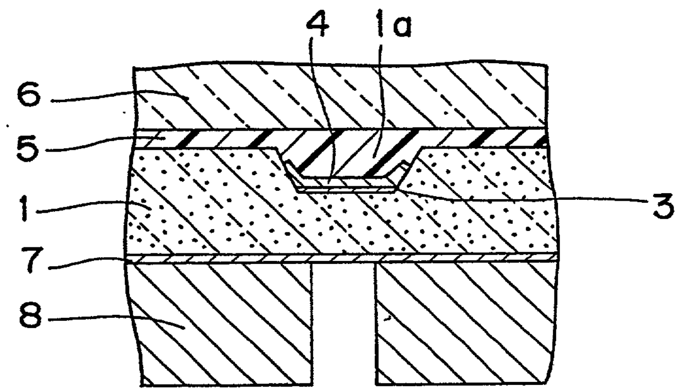

Fig. ~~2~~1H

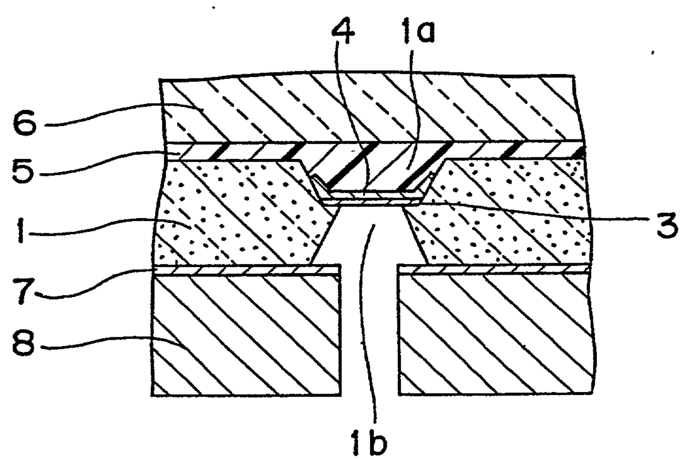

Fig. 3I

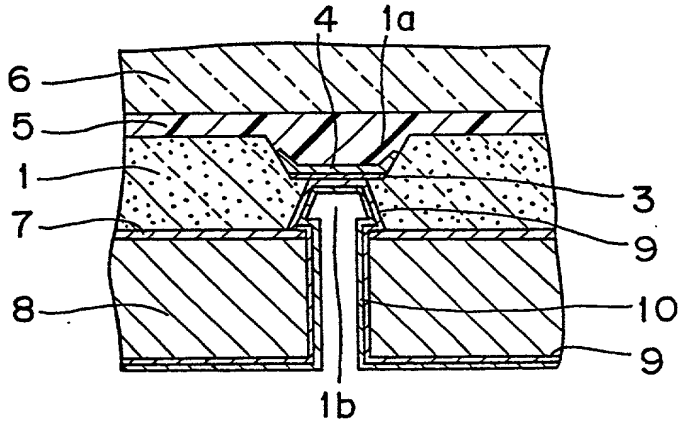

Fig. 3J

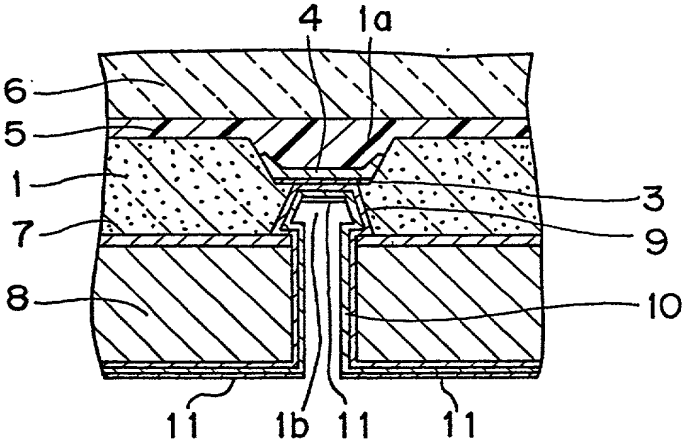

Fig. 3K

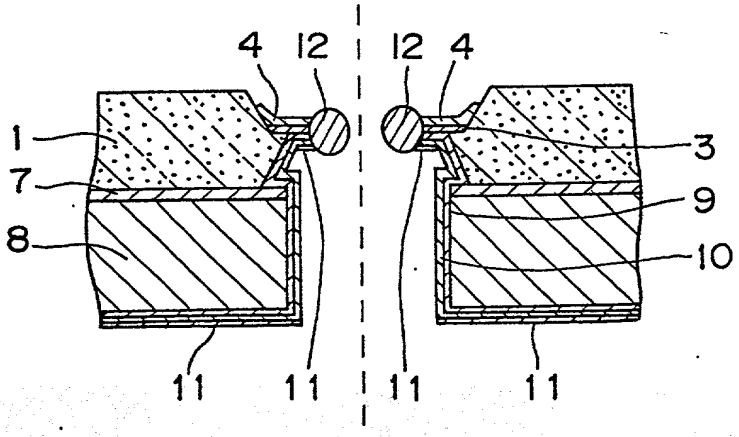

Fig. 4A

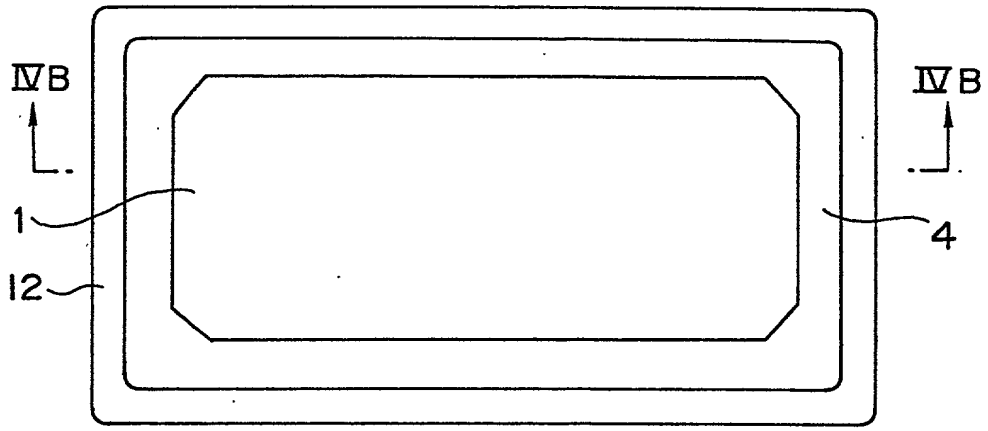

Fig. 4B

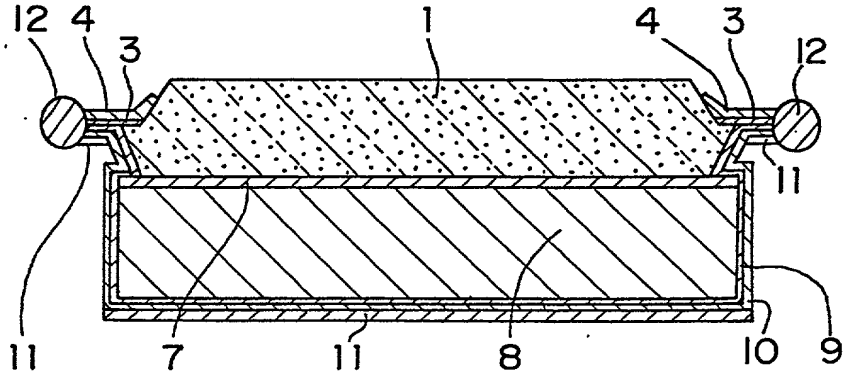

Fig. 3A

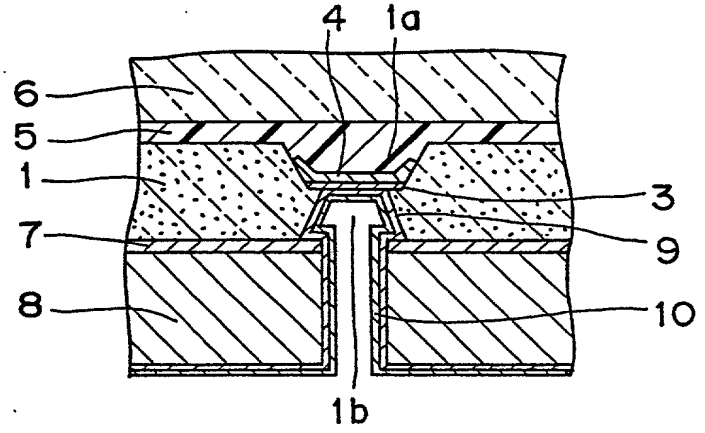

Fig. 3B

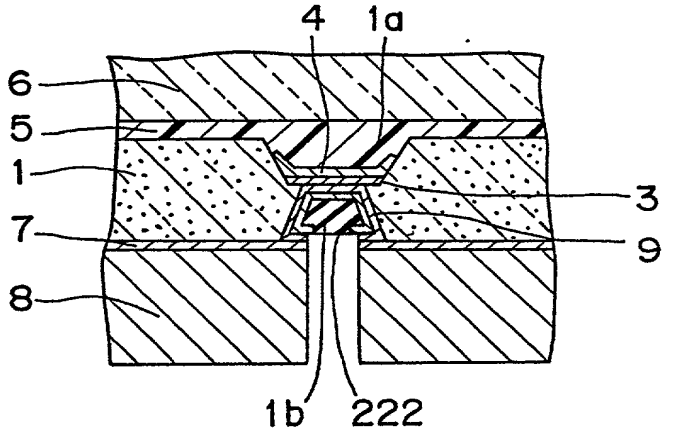

Fig. 3C

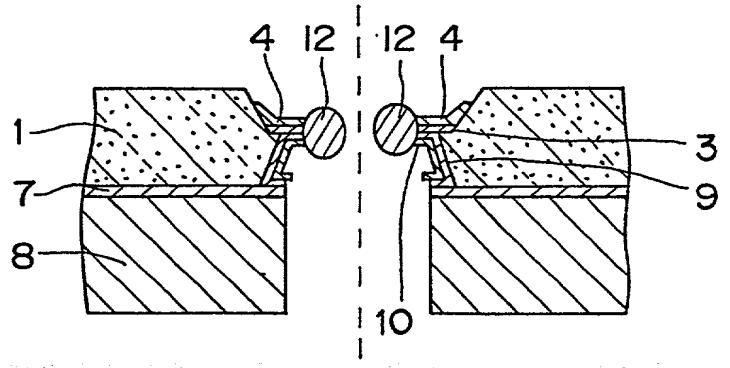

Fig. 6

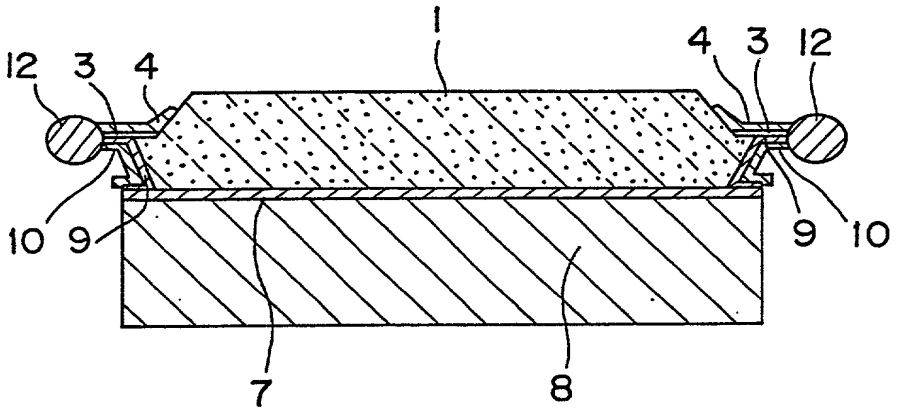

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Fig. 7A PRIOR ART

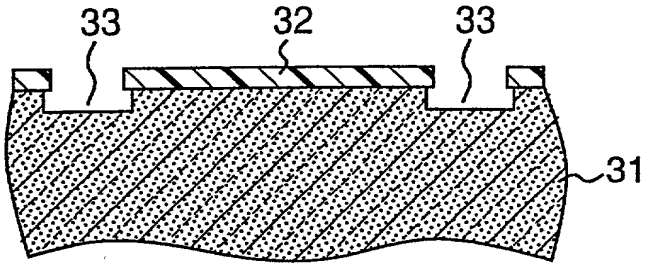

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Fig. 7B PRIOR ART

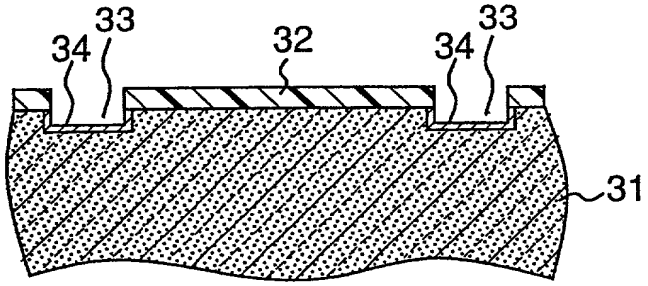

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Fig. 7C PRIOR ART

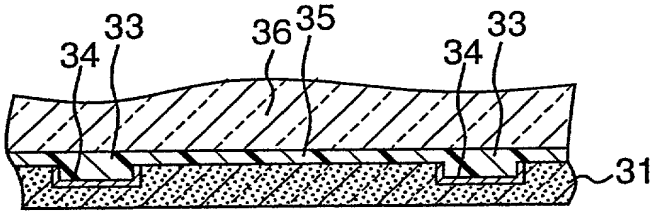

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Fig. 7D PRIOR ART

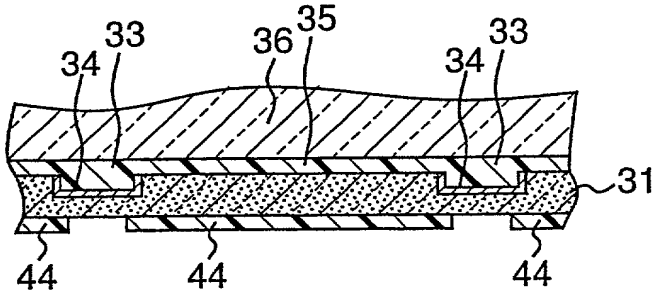

Fig.8E PRIOR ART

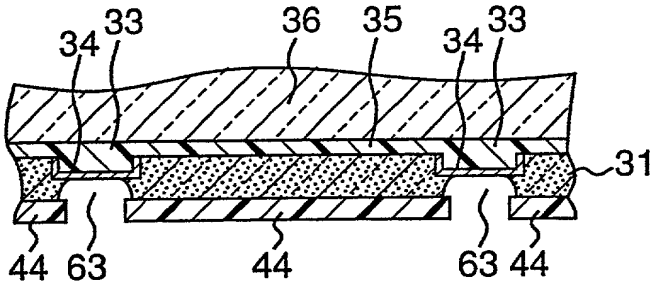

Fig.8F PRIOR ART

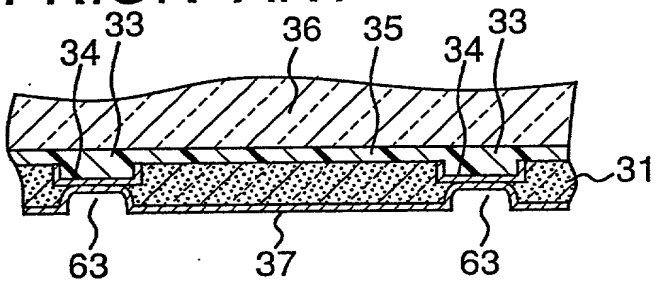

Fig.8G PRIOR ART

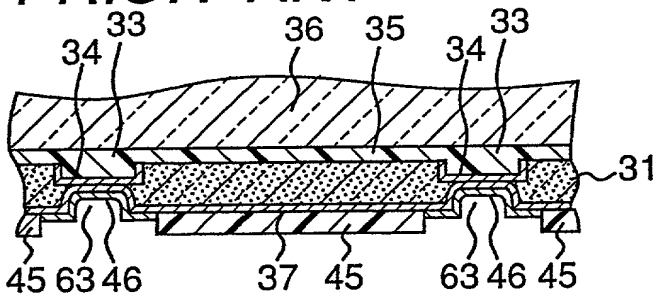

Fig.8H PRIOR ART

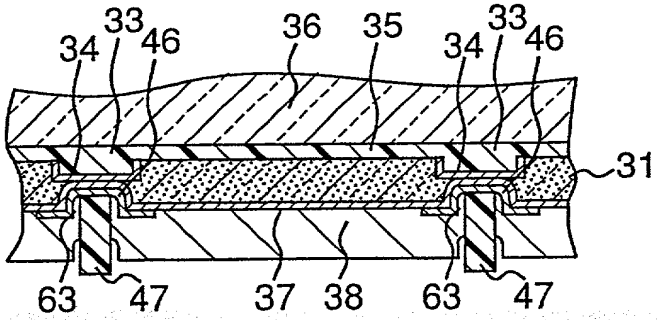

Fig. 9I PRIOR ART

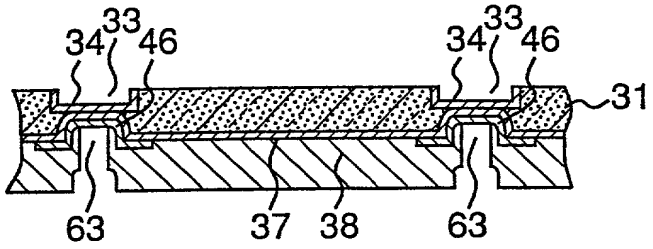

Fig. 9J PRIOR ART

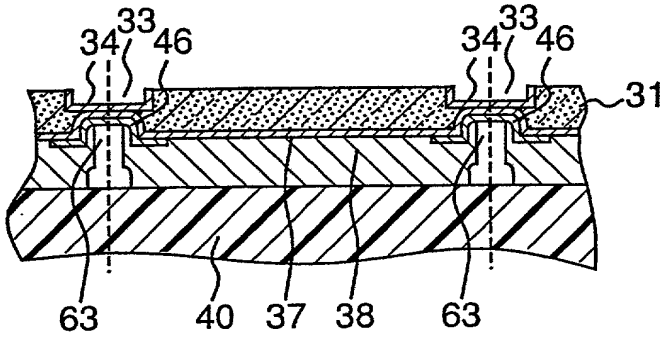

Fig. 9K PRIOR ART

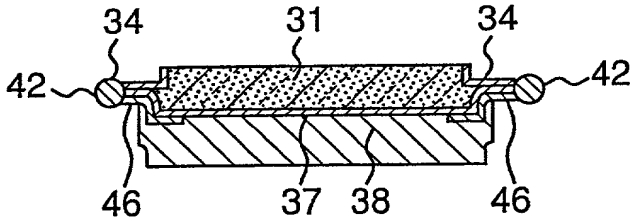

Fig. 9L PRIOR ART